REMARKS

Claims 1-17 are pending.

One embodiment is directed to a circuit 20 for generating a cyclic prefix of a symbol D_t comprised of a sequence of N time samples (Fig. 4). The circuit includes a complex multiplier 22, an inverse fast Fourier transform (IFFT) circuit 12, a FIFO memory 24, and a multiplexer (MUX) 16. The IFFT circuit 12 converts input data from the frequency domain into the N samples in the time domain. The FIFO memory 24 stores some of the N time samples and the MUX combines the stored time samples with samples received directly from the IFFT to produce an output sequence of time samples.

In contrast to prior art circuits, such as the circuit 10 shown in Figure 2, the complex multiplier 22 multiplies the complex coefficients $Aie^{j\varphi i}$ of the input frequency domain signal by respective shifting coefficients $e^{jKi\tau}$. As explained in the paragraph beginning at page 5, line 22, such multiplying by the shifting coefficients amounts to modifying the phase φ_i by a value $\Delta\varphi$, which causes a circular shifting of the corresponding sinusoid section by a value that is a function of the frequency f_i. As a result the current symbol D_t' output by the IFFT circuit 12 corresponds to the preceding symbol D_t having undergone a circular shift by τ samples.

Also in contrast to prior art circuits, the FIFO memory 24 does not need to store all of the time samples, and instead stores only the τ shifted samples. For example, at a first time t_1, the IFFT circuit 12 provides the first sample S_1' of the symbol D_t', the memory 24 stores S_1', and the MUX 16 selects the output of the IFFT to output S_1'. This configuration remains unchanged until a time t_τ such that samples S_1'- S_J' are output by the MUX 16 and stored in the memory 24 (see page 6, lines 23-27). From time $t_{\tau+1}$ to time t t_N, the memory 24 is deactivated whiles the MUX 16 outputs the samples S_{J+1}' to S_N' (page 6, lines 28-31). At time t_{N+1}, the IFFT circuit 12 is stopped and the MUX selects the output of the memory 24 such that the stored samples S_1'- S_J' are output by the MUX until a time $t_{N+\tau}$ (page 7, lines 1-5).

Claims 5, 10, 15, and 17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner questioned the means of "the memory stores only the shifted samples without storing any samples of the symbol other than the shifted samples."

The applicants respectfully submit that claims 5, 10, 15, and 17 are not indefinite. The questioned language of these claims are supported by Figure 4 and the accompanying discussion as summarized above. In Figure 4, the FIFO memory 24 stores only the shifted samples S1'-SJ' without storing the unshifted samples S_{J+1}' to S_N' of the symbol D_t'. Thus, the claim language of claims 5, 10, 15, and 17 reads directly on the exemplary embodiment shown in Figure 4. Accordingly, claims 5, 10, 15, and 17 particularly point out and distinctly claim the invention.

Claims 1, 3-6, 8-11, and 13-17 were rejected under 35 U.S.C. § 102(e) as being anticipated by the applicants admitted prior art (AAPA).

The AAPA does not disclose the invention recited in claim 1. Claim 1 recites a circuit that includes "means for shifting the phase of each complex coefficient by a value proportional to its frequency, so that said last samples of the symbol are shifted at the beginning of the symbol according to a circular permutation." The AAPA does not disclose any means for shifting the phase of each complex coefficient by a value proportional to its frequency. As discussed above, in the embodiment of Figure 4, the complex multiplier 22 performs such a shifting of phase of each complex coefficient by a value proportional to its frequency. The prior art arrangement in Figures 1-2 does not include such a complex multiplier 22 or any other means for shifting the phase of each complex coefficient. The Examiner appears to have missed that language of claim 1 as there is no mention of such phase shifting anywhere in the Background section of the present application. Accordingly, claim 1 is not anticipated by the AAPA.

Claims 3-5 depend on claim 1, and thus, are also not anticipated by the AAPA. In addition, the AAPA does not disclose the features recited in claim 5. As discussed above, claim 5 recites that the memory stores the shifted samples without storing any of the samples other than the shifted samples. As discussed above, in the exemplary embodiment of Figure 4, the memory 24 stores only the shifted samples S1'-SJ' without storing the unshifted samples S_{J+1}' to S_N' of the symbol D_t'. In contrast, the memory 14 of the prior art Figure 2 stores all of the samples S_1 to S_N rather than just the shifted samples S_1 to S_I. Accordingly, claim 5 is not anticipated by the AAPA.

Although the language of claims 6, 8-11, and 13-17 is not identical to that of claims 1 and 3-5, the allowability of claims 6, 8-11, and 13-17 will be apparent in view of the above discussion.

Claims 2, 7, and 13 were rejected under 35 U.S.C. § 103 as being unpatentable over the AAPA in view of U.S. Patent No. 6,574,283 to Sakoda et al. ("Sakoda").

Claim 2 is nonobvious over the AAPA in view of Sakoda. In particular, Sakoda does not teach or such the features of claims 1, from which claim 2 depends, that are missing from the AAPA. The Examiner points to item 22 of Fig. 8 of Sakoda, by item 22 does not shift the phase of each complex coefficient by a value proportional to its frequency. Instead, item 22 is a random phase shift circuit. As its name implies, the random phase shift circuit 22 outputs phase data having random values (see col. 8, lines 36-45). As is well known, such random values by definition cannot be values proportion to a frequency. Thus, the combination of the AAPA and Sakoda is still lacking the "means for shifting the phase of each complex coefficient by a value proportional to its frequency."

In addition, the cited prior art does not teach or suggest the elements recited in claim 2. Claim 2 recites that the shifting means includes "a multiplier connected to multiply each complex coefficient by a complex value having a unity norm and a phase proportional to the frequency associated with each coefficient." Neither the AAPA nor Sakoda suggests such a multiplier that multiples each complex coefficient by a complex value having a unity norm and a phase proportional to the frequency associated with each coefficient. Sakoda shows a multiplier 22B of the random phase shift circuit 22, but does not multiply anything by a complex value having a unity norm and a phase proportional to the frequency associated with each coefficient. Instead, the multiplier 22B "sequentially multiplies the complex sequence in the input transmission signal S20 by the complex sequence in the phase data S21A to randomly vary the phase of the transmission symbol S20" (col. 7, lines 38-41). As discussed above, such random phase data is random rather than proportional to a frequency. Accordingly, it would not be obvious to combine the AAPA and Sakoda to obtain the multiplier recited in claim 2.

For the foregoing reasons, claim 2 is nonobvious in view of the AAPA and Sakoda.

Although the language of claims 7 and 12 is not identical to that of claim 2, the allowability of claims 7 and 12 will be apparent in view of the above discussion.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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